REMARKS

This is an amendment under 37 CFR §1.116. The purpose of this amendment is to put the claims in condition for allowance or, alternately, in better form for appeal. The amendments and specific arguments herein, to the extent they were not presented earlier, are now presented because they are necessitated by the reference citations and arguments made by the Examiner in the last office action.

Since this response is being filed with two months of the mailing date of the final rejection, the courtesy of an advisory action is respectfully requested. Claims 1, 2, 5-7, 9-10, 13-17, and 19-23 are in this application. Claim 18 has been cancelled. Claim 22 has been amended to be in independent form. Claims 19, 21, and 23 have been amended to depend from claim 22. Claim 20 has been amended to correct an inadvertent error. Thus, it is submitted that these amendments do not raise new issues and do not require any further searching.

The Examiner objected to the amendment filed on March 25, 2002 under 35 U.S.C. §132 as introducing new matter. The Examiner also rejected claims 1, 2, 5-7, 9, 10, and 13-17 under 35 U.S.C. §112, first paragraph. In both cases, the Examiner objected to the addition of the phrase "without changing the slurry," arguing that there is no support in the specification for this limitation.

Applicant's specification teaches:

> "Oxide layer 330 and polysilicon layer 320 are chemically-mechanically polished with a slurry that ideally has a selectivity of 1:1 (removes oxide layer 330 at the same rate as polysilicon layer 320)." (See page 6, lines 25-29.)

Thus, applicant's specification teaches that layers 330 and 320 are polished with one slurry. If layers 330 and 320 are polished with one slurry, then layers 330 and 320 must have been polished without changing the slurry. As a result, applicant's specification indirectly teaches that layers 330 and 320 are polished without changing the slurry.

Applicant is unaware of any requirement that claim limitations can only be supported by the express teachings of the specification. Thus, since applicant's specification indirectly teaches that layers 330 and 320 are polished without changing the slurry, applicant's

specification satisfies the requirements of 35 U.S.C. §132, and claims 1, 2, 5-7, 9, 10, and 13-17 satisfy the requirements of the first paragraph of section 112.

The Examiner objected to claim 16 because claim 16 depended from a cancelled claim. Claim 16 has been amended to correct this inadvertent error.

The Examiner rejected claim 20 under 35 U.S.C. §112, first paragraph. Specifically, the Examiner argued that there is no quantitative measurement that indicates that the structure has a minimum thickness range.

Claim 20 recites, in part,

> "wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a value that is equal to or greater than the thickness."

(Claim 20 was amended to remove the inadvertent inclusion of the word minimum.)

The Examiner also rejected claims 5, 13, and 20 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 5 and 13 are similar to claim 20, and recite, in part,

> "wherein the planarized layer of material has a thickness over the wafer upper level, and
> "wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a value that is equal to or greater than the thickness."

In rejecting the claims, the Examiner argued that the "wherein the layer of first material" phrase lacks clarity.

Applicant's specification teaches:

> "When the structures are formed, the structures are specified to have a thickness over the upper levels 314 that ranges from a minimum thickness to a maximum thickness. To achieve this result, polysilicon layer 320 is deposited to have a thickness such that lower level 322 is above upper level 314 by an amount which is at least as great as the minimum specified thickness of the resulting structure." (See page 6, lines 4-9.)

The layer of first material can be read to be, for example, polysilicon layer 320, while the first lower level can be read to be, for example, a lower level 322. In addition, the wafer upper level can be read to be, for example, an upper level 314, while the thickness can be read to be, for example, the minimum specified thickness. (See also the example on page 6, lines 10-19 of applicant's specification.)

Thus, from what applicant can determine, claim 20 satisfies the requirements of the first paragraph of section 112, and claims 5, 13, and 20 satisfy the requirements of the second paragraph of section 112.

The Examiner rejected claims 1, 2, 6, 7, 14-16, 18, 19, 21 and 23 under 35 U.S.C. §102(b) as being anticipated by Doan et al. (U.S. Patent No. 5,618,381). The Examiner also rejected claims 9 and 17 under 35 U.S.C. §103(a) as being unpatentable over Doan et al. Applicant has not addressed the rejections of claims 1, 2, 6, 7, 9 and 14-17 as the Examiner has not, from what applicant can determine, added any new arguments or responded to any of applicant's previous arguments of patentability.

Applicant notes that the Examiner indicated that applicant's arguments with respect to claims 1, 2, 5-7, 9, 10, 13-23 have been considered but are moot in view of the new ground(s) of rejection. However, the Examiner must address any arguments presented by the applicant which are still relevant to any references being applied. (See MPEP §707.07, Examiner Note to Form Paragraph 7.38.)

Thus, it is unclear to applicant whether the Examiner has dropped the Doan rejections, or whether the Examiner inadvertently omitted to address applicant's arguments with respect to Doan. As a result, applicant has not addressed the rejections of claims 1, 2, 6, 7, 9 and 14-17. In addition, as noted above, claim 22 has been amended to be in independent form, and claims 19, 21, and 23 have been amended to depend from claim 22. (Claim 22 was not rejected over Doan.)

The Examiner also rejected claims 1, 2, 5-7, 10, 13-16, and 18-23 under 35 U.S.C. §102(e) as being anticipated by Li et al. (U.S. Patent No. 6,162,368). For the reasons set forth below, applicant respectfully traverses this rejection.

In rejecting the claims, the Examiner argued, citing from column 4, line 37 to column 6, line 54, that Li teaches that the layer of second material (oxide layer 18) is all removed

from the layer of first material (polysilicon layer 16) without changing the slurry to form the planarized layer of material.

Applicant notes that from column 5, line 64 to column 6, line 3, Li teaches:

> "As shown by FIGs. 2B and 2C, the brief polishing at polishing station 25a with oxide-polishing slurry 50a is sufficient to remove native oxide layer 18 from the substrate surface.
> "Referring to FIGs. 2C and 2D, once the native oxide layer has been removed, the substrate is polished with polysilicon-polishing slurry 50b."

Thus, oxide layer 18 (the second layer of material) is removed without changing the slurry. Claim 1 also requires, however, that the polish form a planarized layer of material. As shown in FIGs. 2B and 2C of Li, the brief polish removes oxide layer 18 with the same slurry, but leaves the very non-planar surface of poly layer 16. Thus, Li fails to teach a polish that removes the second layer of material with the same slurry that leaves a planarized layer. As a result, claim 1 is not anticipated by the Li et al. reference. In addition, since claims 2, 5-7, 10, 13-16 either directly or indirectly depend from claim 1, these claims are also not anticipated by Li for the same reasons as claim 1.

Claim 22 recites, in part,

> "chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form a planarized layer of first material, the planarized layer of first material covering the wafer upper level of the top surface of the wafer; and
> "forming a layer of third material on the planarized layer of first material."

In rejecting claim 22, the Examiner did not identify the structure the Examiner was reading to be the "wafer upper level" or the "layer of third material." However, since the Examiner read the first layer of material in claim 1 to be polysilicon layer 16 shown in FIG. 2D of Li, applicant assumes the Examiner is reading the wafer upper level to be the top surface of an insulative layer 14.

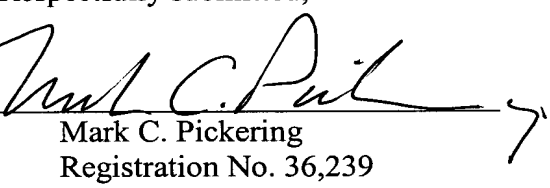
Although applicant is unclear as to what the Examiner is reading to be the third layer of material, it does not matter because Li teaches that it is not possible for a third layer of material to be formed on the planarized layer of material when the planarized layer of material covers the wafer upper level. As shown in FIG. 2D, Li teaches that a planarized

layer of oxide layer 16 is present over the top surface of insulative layer 14 at one point during the fabrication process.

However, as shown in FIG. 2E, the process continues by removing oxide layer 16 from over the top surface of insulative layer 14. As a result, it is not possible for a third layer of material to be formed on planarized oxide layer 16 when planarized oxide layer 16 covers the wafer upper level (the top surface of insulative layer 14). Thus, since Li does not teach that a third layer of material is formed over polysilicon layer 16 while polysilicon layer 16 covers the top surface of insulative region 14, claim 22 is not anticipated by Li. In addition, since claims 19-21 and 23 depend directly or indirectly from claim 22, claims 19-21 and 23 are patentable over Li for the same reasons as claim 22.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

Dated: 11-1-02 By: 

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APPENDIX

In the Claims

Please cancel claim 18.

Please amend the claims as follows:

16. (Amended) The method of claim [3] 1 wherein the layer of first material makes an electrical contact with a device on the wafer.

19. (Amended) The method of claim [18] 22 wherein the first lower level lies above the wafer upper level.

20. (Amended) The method of claim 19

wherein the planarized layer of first material has a thickness over the wafer upper layer, and

wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a value that is equal to or greater than the [minimum] thickness.

21. (Amended) The method of claim [18] 22 wherein the first material is doped polysilicon.

22. (Amended) [The method of claim 18 and further comprising the step of] A method of planarizing a layer of semiconductor material on a processed wafer, the wafer having a top surface, the top surface having a wafer lower level and a wafer upper level that lies above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material; and

chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form a planarized layer of first material, the planarized layer of first material covering the wafer upper level of the top surface of the wafer; and

forming a layer of third material on the planarized layer of first material.

23. (Amended) The method of claim [18] 22 wherein the layer of first material makes an electrical contact with a device on the wafer.